1. A circuit for a voltage controlled oscillator having a timing control by a bias circuitry and having a low phase-noise comprising:

a first pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said pair is connected to the drain of a second transistor of said pair and the base of a second transistor of said pair is connected to the drain of said first transistor of said pair of transistors, the sources of said transistors are connected to each other and to a V_{dd} voltage, and the drain of a first transistor of said first pair of transistors is connected to the drain of a first transistor of a second pair of transistors and the drain of a second transistor of said first pair of transistors is connected to the drain of a second transistor of said second pair of transistors;

a power supply supplying said V_{dd} voltage;

a second pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said second pair is connected via a means of a bias circuitry influencing timing control to the drain of a second transistor of said second pair and the base of a second transistor of said pair is connected via said means of a bias circuitry influencing timing control to the drain of said first transistor of said pair, each base is connected to said means of a bias circuitry influencing timing control, the sources of said pair of transistors are connected to each other and to a current source, and each drain of said transistors is connected to a means of a LC-tank;

a means of a bias circuitry influencing timing control;